CLAIMS

What is claimed is:

1. A current sense circuit comprising:

first and second transistors, each having first and second terminals and a control terminal, the conduction through each transistor between the first and second terminals being controlled by the voltage between the control terminal and the first terminal of the respective transistor;

the first transistor having its first and second terminals configured to connect in series with a first power supply terminal and a load;

the first terminal of the second transistor being connected to the first terminal of the first transistor, and the control terminal of the second transistor being connected to the control terminal of the first transistor;

first biasing circuitry biasing the first and second transistors to operate with equal first to second terminal voltages;

a first control loop responsive to a reference voltage to clamp the first to second terminal voltages of the first and second transistors to a predetermined voltage; and,

a second control loop providing a sense circuit output current linearly varying with the current through the second transistor.

2. The current sense circuit of claim 1 where the second control loop has a high output impedance.

3. The current sense circuit of claim 1 wherein the first transistor is N times larger than the second transistor, wherein N is substantially greater than one.

4. The current sense circuit of claim 3 wherein the second control loop provides a sense circuit output current component equal to the current through the second transistor minus a bias current on the second transistor.

5. The current sense circuit of claim 4 further comprised of second biasing circuitry biasing the sense circuit output current to a zero current when a load current is zero.

6. The current sense circuit of claim 1 wherein the second control loop is not active when the voltage on the load connection to the first transistor approaches the voltage of a second power supply terminal, and further comprising a third control loop, the third control loop providing a sense circuit output current linearly varying with the current through the second transistor when the voltage on the load connection to the first transistor approaches the voltage of a second power supply terminal.

7. The current sense circuit of claim 6 further comprising:

a second current sense circuit comprising:

third and fourth transistors, each having first and second terminals and a control terminal, the conduction through each transistor between the first and second terminals being controlled by the voltage between the control terminal and the first terminal of the respective transistor;

the third transistor having its first and second terminals configured to connect in series with a second power supply terminal and a load;

the first terminal of the fourth transistor being connected to the first terminal of the third transistor, and the control terminal of the fourth transistor being connected to the control terminal of the third transistor;

first biasing circuitry biasing the third and fourth transistors to operate with equal first to second terminal voltages;

a first control loop responsive to a reference voltage to clamp the first to second terminal voltages of the third and fourth transistors to a predetermined voltage; and,

a second control loop providing a sense circuit output current linearly varying with the current through the fourth transistor; and,

a third current sense circuit comprising:

fifth and sixth transistors, each having first and second terminals and a control terminal, the conduction through each transistor between the first and second terminals being controlled by the voltage between the control terminal and the first terminal of the respective transistor;

the fifth transistor having its first and second terminals configured to connect in series with a first power supply terminal and a load;

the first terminal of the sixth transistor being connected to the first terminal of the fifth transistor, and the control terminal of the sixth transistor being connected to the control terminal of the fifth transistor;

first biasing circuitry biasing the fifth and sixth transistors to operate with equal first to second terminal voltages;

a first control loop responsive to a reference voltage to clamp the first to second terminal voltages of the fifth and sixth transistors to a predetermined voltage; and,

a second control loop providing a sense circuit output current linearly varying with the current through the second transistor;

the output of the current sense circuit of claim 5 being coupled to flow between the first and second terminals of the third transistor, the output of the second current sense circuit being coupled to flow between the first and second terminals of the third current sense output.

8. The current sense circuit of claim 7 wherein the first power supply terminal is a positive power supply terminal and the second power supply terminal is a negative power supply terminal relative to the positive power supply terminal.

9. The current sense circuit of claim 7 further comprised of a resistor coupled to the output of the third current sense circuit output.

10. A current sense system operating between first and second power supply terminals comprising:

a first current sense circuit coupled between the first and second power supply terminals and having a first current sense input and a first current sense output, the first current sense circuit providing a current sense output current proportional to the current in the first current

sense input when the voltage on the first current sense input is between the voltages on the first and second power supplies;

a second current sense circuit coupled between the first and second power supply terminals and having a second current sense input coupled to the first current sense output, and a second current sense output, the second current sense circuit providing a second current sense output current proportional to the current in the second current sense input while holding the voltage between the second current sense input and the second power supply terminal constant; and,

a third current sense circuit coupled between the first and second power supply terminals and having a third current sense input coupled to the second current sense output, and a third current sense output, the third current sense circuit providing a third current sense output current proportional to the current in the third current sense input while holding the voltage between the second current sense input and the first power supply terminal constant.

11. A method of sensing current using transistors, each having first and second terminals and a control terminal, the current flow between the first and second terminals being controlled by the voltage between the control terminal and the first terminal, comprising:

coupling the first and second terminals of the first transistor in series with a source of power and a load;

using a first control loop responsive to a set voltage, mirroring a current proportional to the current through the first transistor to a second transistor while maintaining the voltages between the control terminal and the first terminal of the first and second transistors equal, and also maintaining the voltages between the first and second terminals of the first and second transistors equal; and,

providing a current sense output responsive the current between the first and second terminals of the second transistor.

12. The method of claim 11 wherein the current sense output is provided by a second control loop, the second control loop providing a current sense output current changing linearly with and equal to changes in current between the first and second terminals of the second transistor.

13. The method of claim 12 further comprised of including a bias current in the current sense output current to make the current sense output current equal to zero when the load current is zero.

14. A method of current sensing comprising:

passing the current to be sensed through a transistor;

controlling the transistor so that the voltage drop across the transistor is independent of the current to be sensed; and,

providing an output responsive to the current in the transistor.

15. The method of claim 14 wherein the output is proportional to the current in the transistor.

16. The method of claim 15 wherein the output is a current.

17. The method of claim 14 further including replicating the current in the transistor to provide a replica current proportional to the current in the transistor, and wherein providing an output responsive to the current in the transistor comprises providing an output responsive to the replica current.

18. The method of claim 14 wherein the transistor is a FET.

19. A method of current sensing comprising:

providing first and second transistors, the first transistor being N times the size of the second transistor;

passing the current to be sensed through the first transistor;

controlling the first and second transistors so that the voltages across the first and second transistors are equal to a reference voltage and independent of the input current to replicate the current in the first transistor in the second transistor in a ratio of 1/N; and,

providing an output that varies linearly with the current in the second transistor.

20. The method of claim 19 wherein the first and second transistors are biased by bias current sources.